REMARKS

This paper is in response to the official action dated October 15, 2002. Claims 1-5 are pending.

Figs. 1A-1D and Fig. 3 have been amended to be designated "prior art" and Figs. 4A-4D have been added to describe the disclosure (Figs. 4A-4D) and the prior art (Figs. 1A-1D, and Fig. 3) using different drawings.

Claim 1 has been objected to because of the expression "a spacer" after the term "etching". Claim 1 has been amended in view of the examiner's comments. Also, claim 1 has been amended to more clearly emphasis the characteristics of the invention.

Claims 1-5 have been rejected as anticipated (claim 1) or obvious over Harakawa, JP 07-183513, either taken alone (claims 3 and 5) or in combination with Beinglass et al., U.S. 5,932,286 (claims 2 and 4). These rejections are respectfully traversed in view of the following.

The application discloses forming a polysilicon layer on an insulating film formed on a semiconductor substrate, forming a metal layer on said polysilicon layer, depositing a nitride film on said metal layer by a low-pressure chemical vapor deposition method to form a hard mask layer,. patterning said hard mask layer to form a patterned hard mask, patterning said metal layer and said polysilicon layer using the patterned hard mask to form a patterned metal layer, and depositing a nitride film by a low-pressure chemical vapor deposition method and then etching to form a spacer at a sidewall of the patterned metal layer, the patterned polysilicon layer, and the patterned hard mask.

Harakawa does not teach or suggest about using a patterned hard mask to form a patterned metal layer. Referring to the paragraph of [0012] in the specification of Harakawa, the following contents is stated: "Etching processing is given as it is shown in drawing 3, using this resist pattern as a mask. That is, using reactive ion etching (RIE) silicon nitride 106 and the tungsten silicide film 105 are processed into a gate electrode configuration, and

resist is removed." Thus, Harakawa appears to disclose using the resist pattern as a mask to form the patterned metal layer. Therefore, it appears Harakawa is not silent about using the patterned hard mask to form the patterned metal layer. Also, Harakawa does not disclose using a patterned hard mask to form a patterned polysilicon layer.

Furthermore, Harakawa does not teach forming a spacer at a sidewall of the patterned metal layer, the patterned polysilicon layer, and the patterned hard mask.

Beinglass et al. does not teach using a patterned hard mask to form the patterned metal layer and the patterned polysilicon layer, and forming a spacer at a sidewall of the patterned metal layer, the patterned polysilicon layer, and the patterned hard mask.

Applicant therefore respectfully submits that the rejection of claims 1-5 under the provisions of 35 U.S.C. §§ 102(b) and 103(a) as being unpatentable is improper, since Harakawa and Beinglass et al. do not disclose or suggest the invention. The examiner is therefore respectfully requested to withdraw the rejection of claims 1-5.

Applicant respectfully requests reconsideration and allowance of this application.

Should the examiner with to discuss the foregoing or any manner of form in an effort to advance this application toward allowance, he is urged to telephone the undersigned at the indicated number.

Respectfully submitted,

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By: _____

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning at page 5, line 21 has been changed as follows:

Referring to Fig. [1A] 4A, a gate oxide film 2, a polysilicon layer 3, a metal layer 4 and a hard mask layer 5 are sequentially formed on a semiconductor substrate 1. Then, photolithographic film patterns 6 are formed on the hard mask layer 5. The metal layer 4 is made of metal such as aluminum (Al), tungsten (W) and titanium (Ti) or silicide. The hard mask layer 5 uses a nitride film deposited by low-pressure chemical vapor deposition (LPCVD) using SiH4 and NH3 in a single type chamber capable of processing a wafer one by one. The deposition process includes the following conditions: the temperature is 600°C to 800°C and the pressure is over 1 Torr, preferably, 1 Torr to 500 Torr. Also, the nitride film is formed in a thickness of 500Å to 3000Å.

The paragraph beginning at page 6, line 8 has been changed as follows:

Referring to Fig [1B] 4B, the hard mask layer 5 is patterned by an etch process using the photolithographic film patterns 6 as a mask to form hard masks 5a.

The paragraph beginning at page 6, line 11 has been changed as follows:

By reference to Fig. [1C] 4C, the metal layer 4, the polysilicon layer 3 and the gate oxide film 2 are sequentially patterned by an etch process using the hard masks 5a as a mask to form a gate electrode 4a. Next, an impurity ion is implanted into the semiconductor substrate 1 at both sides of the gate electrode 4a to form a junction region 7.

The paragraph beginning at page 6, line 16 has been changed as follows:

Referring now to Fig. [1D] 4D, a spacer 8 as an insulating film is formed at both sides of the hard mask 5a and the gate electrode 4a. The insulating film for forming the spacer 8

may be formed using a nitride film such as the nitride film used as the hard mask 5a. At this time, the nitride film is formed by a low-pressure chemical vapor deposition (LPCVD) method in a batch type chamber having the pressure of below 1 Torr, preferably 0.1 Torr to 1 Torr. The thickness of the nitride film is 50Å to 1000Å.

IN THE DRAWINGS:

Please enter the following change to the drawing:

Please label Figs. 1A-1D and Fig. 3 with the legend "Prior Art", and add new Figs. 4A-4D.

A request for approval of drawings changes is submitted herewith.

IN THE CLAIMS:

Please amend claim 1 as follows:

1. (Amended) A method of forming wiring in a semiconductor device, comprising the steps of:

forming a [conductive layer] polysilicon layer on an insulating film formed on a semiconductor substrate;

forming a metal layer on said polysilicon layer;

depositing a nitride film on said [conductive layer] metal layer by a low-pressure chemical vapor deposition method to form a hard mask layer ;

patterning said hard mask layer to form a patterned hard mask;

patterning said [conductive layer] metal layer and said polysilicon layer using the patterned hard mask to form a patterned [conductive layer] metal layer and said polysilicon layer; and

depositing a nitride film by a low-pressure chemical vapor deposition method and then etching [a spacer] to form a spacer at a sidewall of the patterned [conductive layer] metal layer, the patterned polysilicon layer and the patterned hard mask.

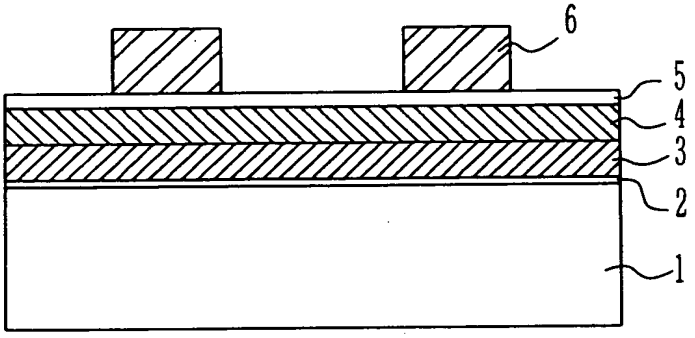

FIG. 1A
(PRIOR ART)

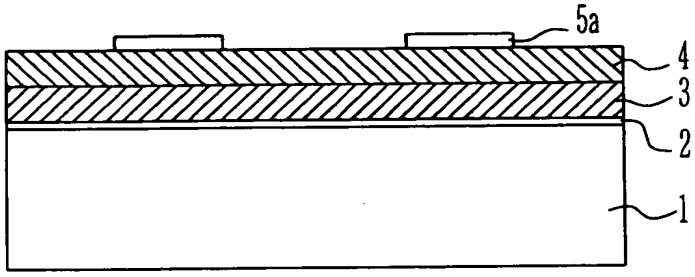

FIG. 1B
(PRIOR ART)

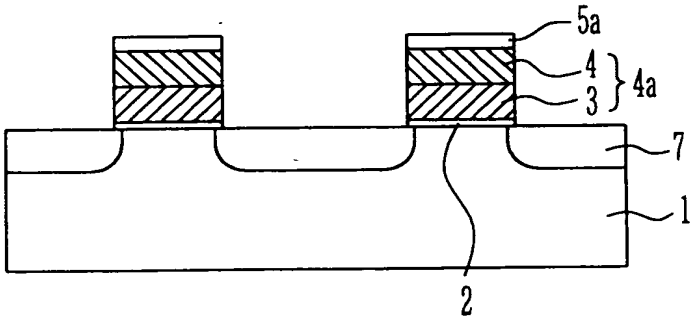

FIG. 1C
(PRIOR ART)

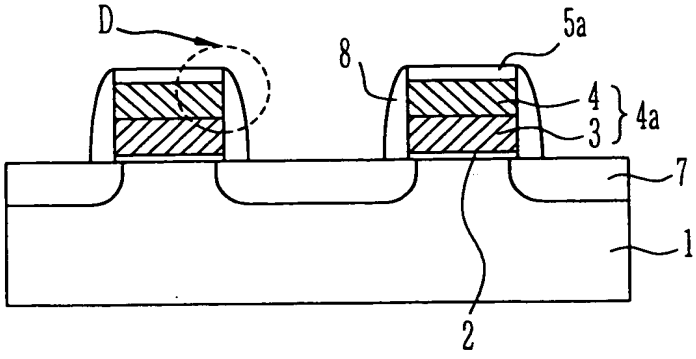

FIG. 1D
(PRIOR ART)

FIG. 2

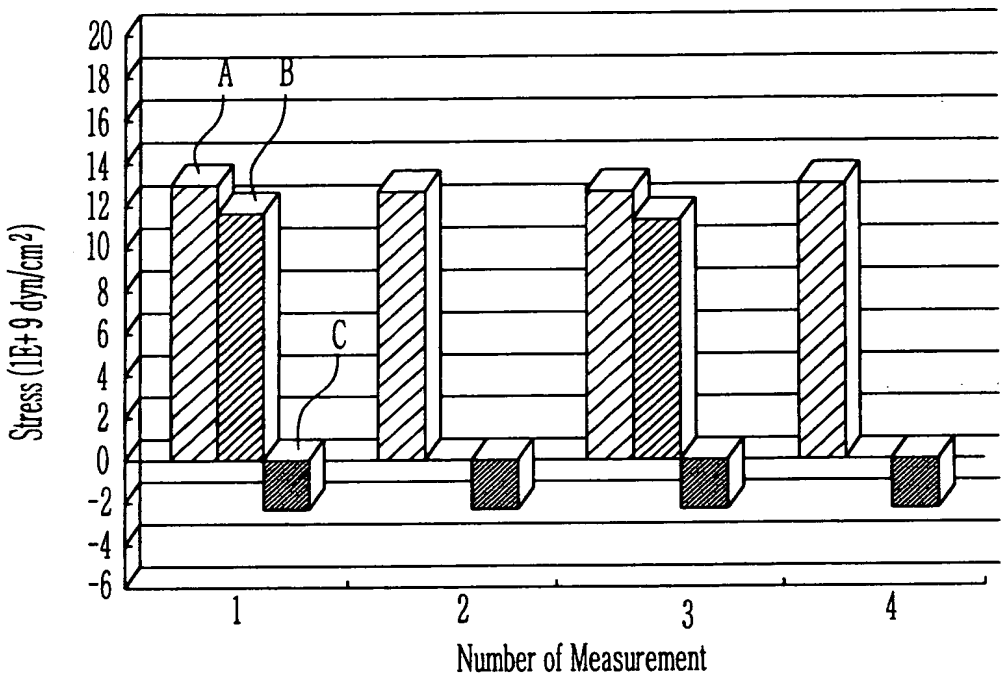

FIG. 3
(PRIOR ART)